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(Not for submission under 37 CFR 1.99)

Application Number	10602292
Filing Date	2003-06-24
First Named Inventor	Michael B. Doerr
Art Unit	2181
Examiner Name	Meonske, Tonia L.
Attorney Docket Number	5860-00101

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	3	4493048		1985-01-08	Kung, et al.	
	4	4807183		1989-02-21	Kung, et al.	
	5	5634043		1997-05-27	Self, et al.	
	6	5805915		1998-09-08	Wilkinson, et al.	
	7	5963746		1999-10-05	Barker, et al.	
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	2	Waingold et al., "Baring It All to Software: Raw Machines," IEEE Computer, September 1997, 8 pages.	<input type="checkbox"/>
	3	Taylor et al., "The Raw Microprocessor: A Computational Fabric for Software Circuits and General-Purpose Programs," IEEE Micro, March-April 2002, 11 pages.	<input type="checkbox"/>
	4	Lee et al., "Space-Time Scheduling of Instruction-Level Parallelism on a Raw Machine," Proceedings of the Eighth International Conference on Architectural Support for Programming Language and Operating Systems (ASPLOS-8), October, 1998, 11 pages.	<input type="checkbox"/>

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TLMD	5	Barua et al., "Compiler Support for Scalable and Efficient Memory Systems," IEEE Transactions on Computers, November 2001, 32 pages.	<input type="checkbox"/>
	6	Lee et al., "Convergent Scheduling," Proceedings of the 35th International Symposium on Microarchitecture (MICRO-35), November 2002, 12 pages.	<input type="checkbox"/>
	7	Babb et al., "Parallelizing Applications into Silicon," Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines '99 (FCCM '99), April 1999, 11 pages.	<input type="checkbox"/>
	8	Babb et al., "The RAW Benchmark Suite: Computation Structures for General Purpose Computing," IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM '97), April 1997, 10 pages.	<input type="checkbox"/>
	9	Babb et al., "Solving Graph Problems with Dynamic Computation Structures," SPIE Photonics East: Reconfigurable Technology for Rapid Product Development & Computing, November 1996, 12 pages.	<input type="checkbox"/>
	10	Frank et al., "SUDS: Primitive Mechanisms for Memory Dependence Speculation," MIT/LCS Technical Memo LCS-TM-591, January 6, 1999, 9 pages.	<input type="checkbox"/>
	11	Barua, "Maps: A Compiler-Managed Memory System for Software-Exposed Architectures," PhD Thesis, MIT Laboratory for Computer Science, January 2000, 161 pages.	<input type="checkbox"/>
	12	Barua et al., "Maps: A Compiler-Managed Memory System for Raw Machines," Proceedings of the Twenty-Sixth International Symposium on Computer Architecture (ISCA-26), June, 1999, 12 pages.	<input type="checkbox"/>
	13	Barua et al., "Memory Bank Disambiguation using Modulo Unrolling for Raw Machines," Proceedings of the Fifth International Conference on High Performance Computing, December, 1998, 9 pages.	<input type="checkbox"/>
	14	Moritz, et al., "Hot Pages: Software Caching for Raw Microprocessors," MIT/LCS Technical Memo LCS-TM-599, August, 1999, 12 pages.	<input type="checkbox"/>
	15	Miller, "Software Based Instruction Caching for the RAW Architecture," Master's Thesis, Massachusetts Institute of Technology, May, 1999, 39 pages.	<input type="checkbox"/>

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TLMD	16	Taylor et al., "How to build scalable on-chip ILP networks for a decentralized architecture," MIT/LCS Technical Memo MIT-LCS-TM-628, April 2000, 15 pages.	<input type="checkbox"/>
	17	Taylor et al., "Scalar Operand Networks: On-chip Interconnect for ILP in Partitioned Architectures," MIT/LCS Technical Report LCS-TR-859, July 2002, 20 pages.	<input type="checkbox"/>
	18	Taylor, "Design Decisions in the Implementation of a Raw Architecture Workstation," Master's Thesis, Massachusetts Institute of Technology, September, 1999, 90 pages.	<input type="checkbox"/>
	19	Moritz et al., "Exploring Optimal Cost-Performance Designs for Raw Microprocessors," Proceedings of the International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 98), April 1998, 16 pages.	<input type="checkbox"/>
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	22	AGARWAL, ANANT, ET AL., "The MIT Alewife Machine", Proceedings of the IEEE, Vol. 87, No. 3, March 1999, pages 430-444.	<input type="checkbox"/>
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	24	KIMELMAN, D. ET AL., "Visualizing the Execution of High Performance Fortran (HPF) Programs", Proceedings of the 9th International Parallel Processing Symposium, Santa Barbara, CA, April 25-28, 1995, IEEE Computer Society, Los Alamitos, CA, April 25, 1995, pages 750-759.	<input type="checkbox"/>

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